Digitally Assisted RF Circuits

EE633-Seminar

Sohaib Afridi
The Dream- “Software Radio”

[Schreier, "ADCs and DACs: Marching Towards the Antenna," GIRAFE workshop, ISSCC 2003]
Reality—"Heat-Sink Radio"

[Schreier, "ADCs and DACs: Marching Towards the Antenna," GIRAFE workshop, ISSCC 2003]
Strategies for evolution of RF circuits in CMOS process

RF Circuits

Reduce Supply Voltage

All-Digital RF Circuits

Digitally-Assisted RF Circuits

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Strategies for evolution of RF circuits in CMOS process

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Supply Voltage reduction

• Exploiting full device characteristics
  – Reverse short-channel effect (RSCE), Body-bias

• Circuit Topologies
  – Eliminate stacks, LCMFB, CMFF.
  – Address leakage (cascaded switches).

• Revision in Architectures

• True low voltage design: no voltage boosting, no special devices
Strategies for evolution of RF circuits in CMOS process

- Reduce Supply Voltage
- All-Digital RF Circuits
- Digitally-Assisted RF Circuits
All-Digital RF Circuits

• All Digital Synthesizer
• All-digital phase-locked loop (ADPLL) comprising: digitally-controlled oscillator (DCO), time-to-digital converter (TDC), and digital loop filter.
• Direct-sampling discrete-time receiver comprising switched-cap circuits that perform various FIR and IIR filter operations
Strategies for evolution of RF circuits in CMOS process

RF Circuits

- Reduce Supply Voltage
- All-Digital RF Circuits
- Digitally-Assisted RF Circuits

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Why use Digital Assistance?

• To self-calibrate RF front-end.
• Achieve tunability at the cost of low power and low area digital gates.
• Possibly replacing any RF functional block with a digital RF block.
Keys to meaningful digitally assisted architectures

• Exploit the superior time-domain resolution of digital edge transitions in advanced CMOS processes.

• Use techniques that will improve with CMOS scaling.

• As always, thoughtful partitioning of functionality between the analog and digital domains. (There are some things that are still best done in analog.)
Notable Researchers

• **Joel L. Dawson**, Massachusetts Institute of Technology, “Digitally Assisted Architectures for RF Transceivers”

• **Boris Murmann**, Stanford University, “Overview of Digital Correction Techniques for High-Speed Data Converters”

• **Larry Larson**, University of California at San Diego, “Digitally Assisted Transmitter Technology for Wireless Transmitters”

• **Robert Bogdan Staszewski**, Associate Professor, Delft University of Technology, “All-digital Transceivers”
Notable Companies and Labs

- **Texas Instruments**, “Software Assisted Radio Design to Compensate for Analog Impairments and for RF Interference Effects”.
- **MIT Lincoln labs**, “Error correcting codes and optimized pulse shaping filters for enhancing the efficiency of power amplifiers”.
- **Analog Devices and MCCI**, “Highly digitized multi-mode RF transceivers and high speed optical communications transceivers”.

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EXAMPLES
Digitally Assisted PA Design

**Mobile Phone Transceiver**

**Problem:** Need the power amplifier to be both linear *and* efficient.
Power efficiency and Linearity

Power efficiency \rightarrow Battery lifetime & Thermal management

Linearity \rightarrow Spectral efficiency
Cartesian feedback to train a pre-distorter!

Keeps modeling simple but BW limited and cannot be applied on wideband signals!

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Digitally assisted Cartesian Feedback - Step 1

Slowly step through all symbols, and fill LUT.

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Digitally assisted Cartesian Feedback- Step 2

- Transmit using open-loop digital predistortion.
- Retrain as needed.

Evolving the architecture

After defining the LUT through the initial calibration the Delta-Sigma modulated predistortion will take its place and predistort all the incoming symbols to the system.
A checklist of benefits

• Exploit CMOS scaling trends.
  – Digital $\Sigma\Delta$ modulators improve with digital device speed.

• Optimally partition functionality between analog and digital domains.
  – Digital does the modeling, but does so by exploiting feedback.

• Use digital to clean up “sloppy” analog?
  – Yes. Use of low-precision D/As simplifies design.
Direct-Conversion FrontEnd with Digitally Assisted IIP2 Calibration

- >40dB IIP2 improvement!
- Performance very stable w.r.t. any changes (VDD, freq., ...)
- Simpler, lower power RF circuits can be used taking advantage of calibration engine
- Low Power, no extra power consumption for RF operation
- 130nm CMOS process area of 1.56mm²

900MHz Receiver with Interference Cancellation

- >20dB of attenuation for out of channel blockers
- Digital calibration of LO phase (Φ) and alt. path gain is key enabler to automatically tune the position of the cancellation notch
- Consumes 26.4mW from a 0.6V, occupies 2.56mm² low power 65nm CMOS process.

Noise Cancelling Amplifier with Frequency Detector and Digital Control

• An LNA fabricated in 0.13um CMOS process.

• Improving the noise figure is fundamental.

• This is accomplished by finding the combinations of bias voltages at various transistor gates that would produce the minimum noise figure at a given frequency while maintaining a specific gain that would be the same at all frequencies.

• Improves Gain flatness by 1GHz and Noise Figure keeps less than 4dB.


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Gilbert Cell Mixer With an off-chip Linear Interpolator as digital assistance

• A Gilbert mixer in 0.13um CMOS process.

• Off-chip microcontroller measures the input power through the RF power detector and based on an earlier linearity sweep decides the bias voltages Gilbert Cell.

• IIP3 improved by 6dB.


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Conclusions

• CMOS Scaling is driving semiconductor technology and will continue for another decade, but with significant design challenges.
• Design is becoming a prime differentiator.
• There are many ways to take advantage of digital circuits:
  – Calibration
  – Digital compensation for analog impairments
  – Clever use of CMOS switches
  – Using “digital” topologies for analog functions
  – Encoding information in timing of digital edges
  – ...and more to come!
THANK YOU
Supply Voltage reduction


All Digital RF Circuits


Digitally Assisted RF